2. INTERFACE DESCRIPTION

2.1. PIN ASSIGNMENTS

The pin assignments for the the 84-pin PLCC and the 80-pin PQFP packages are shown in Figure 2-1. The I/O signals are shown in Figure 2-2 along with the major interfacing MPU functions.

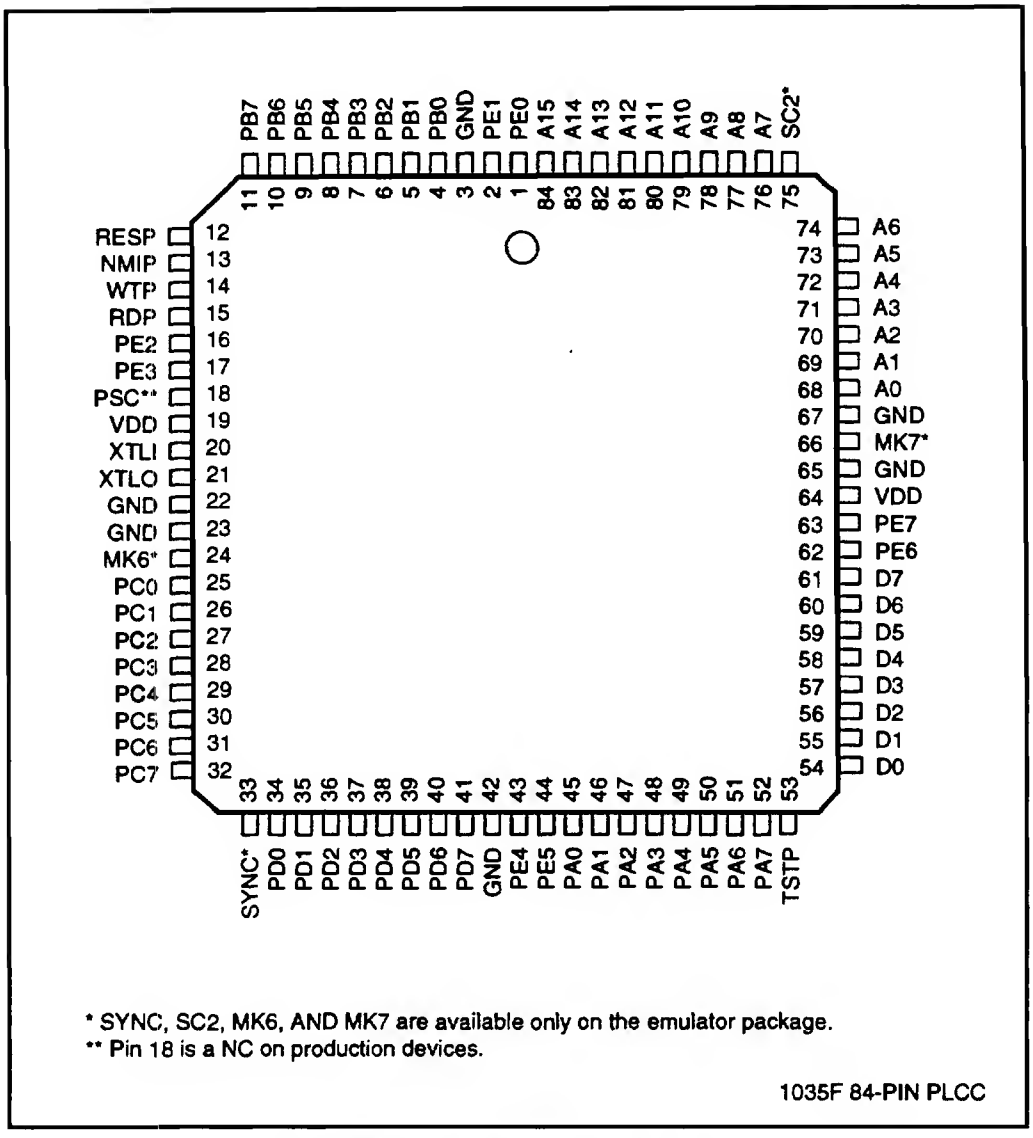

Figure 2-1a. Pin Assignments - 84-Pin PLCC

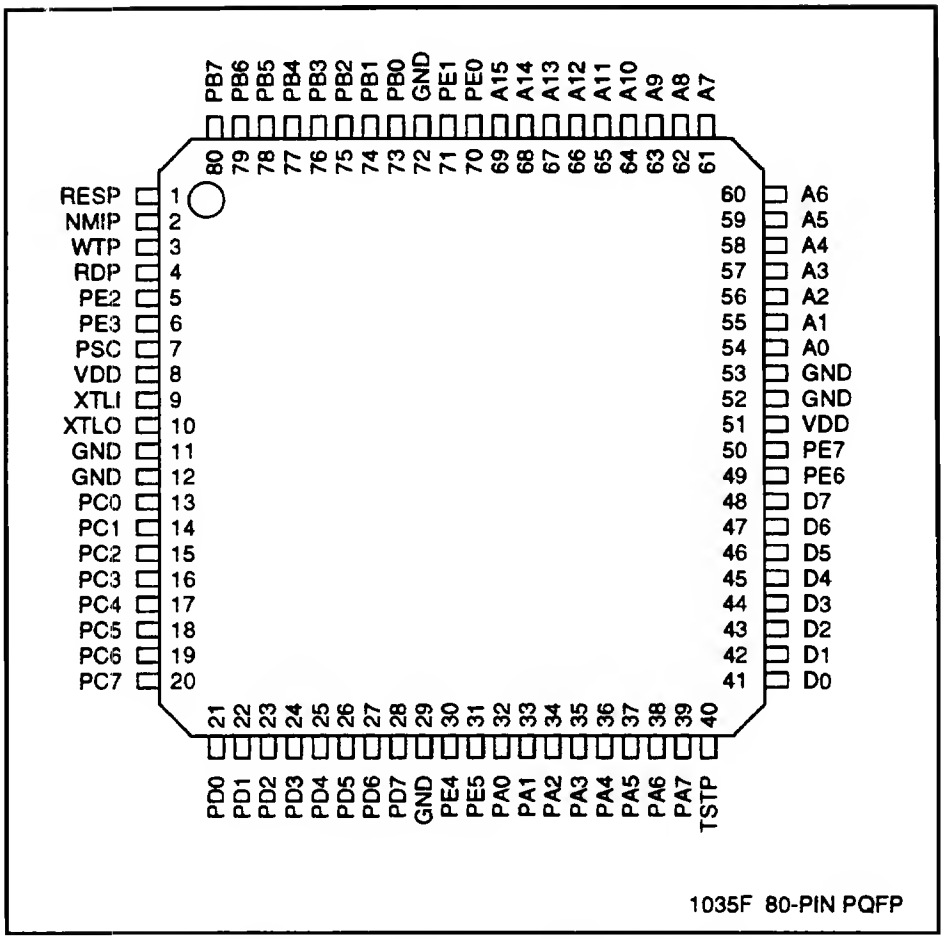

Figure 2-1b. Pin Assignments - 80-Pin PQFP

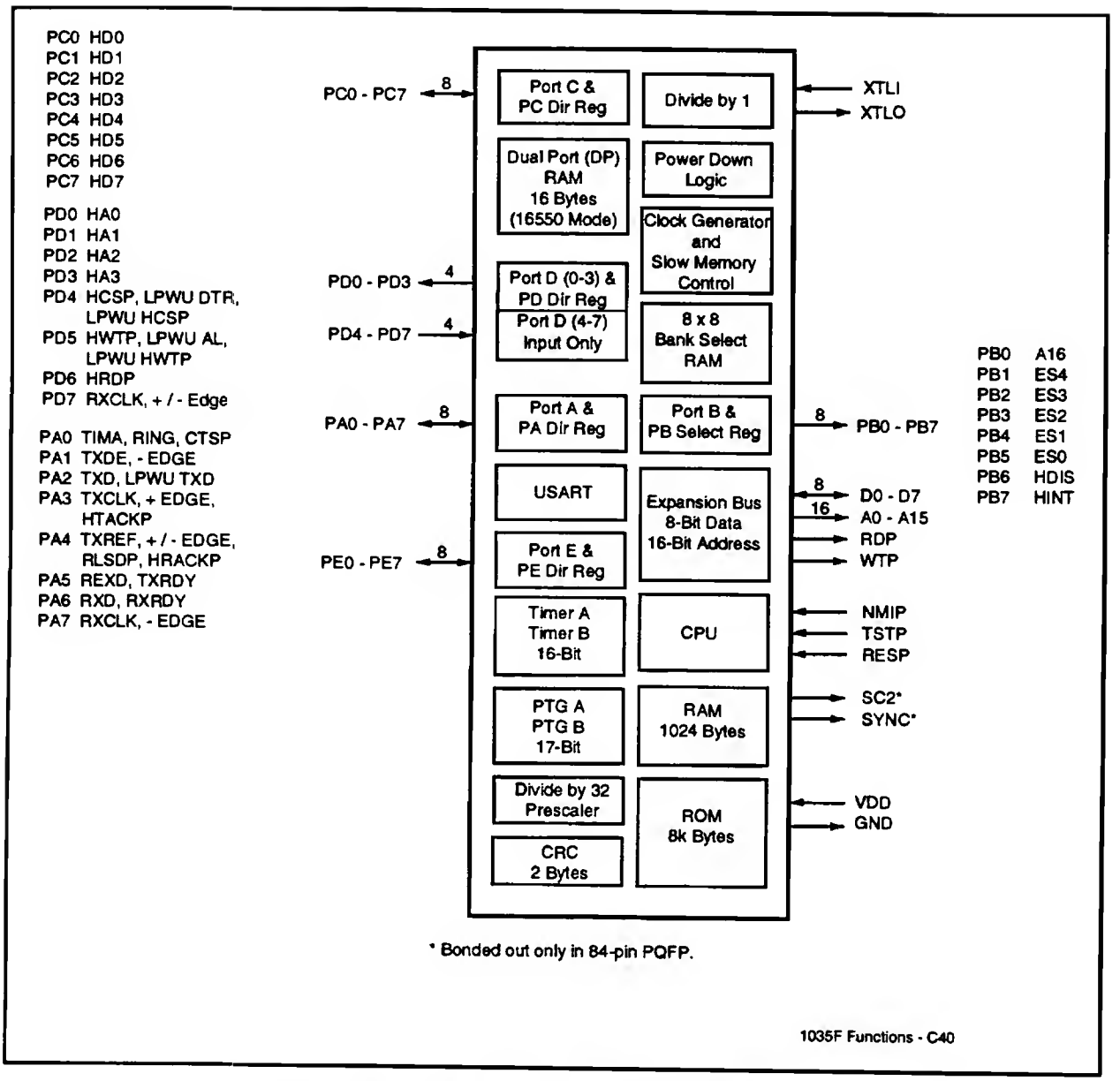

Figure 2-2a. Internal Functions and I/O Signals - C40

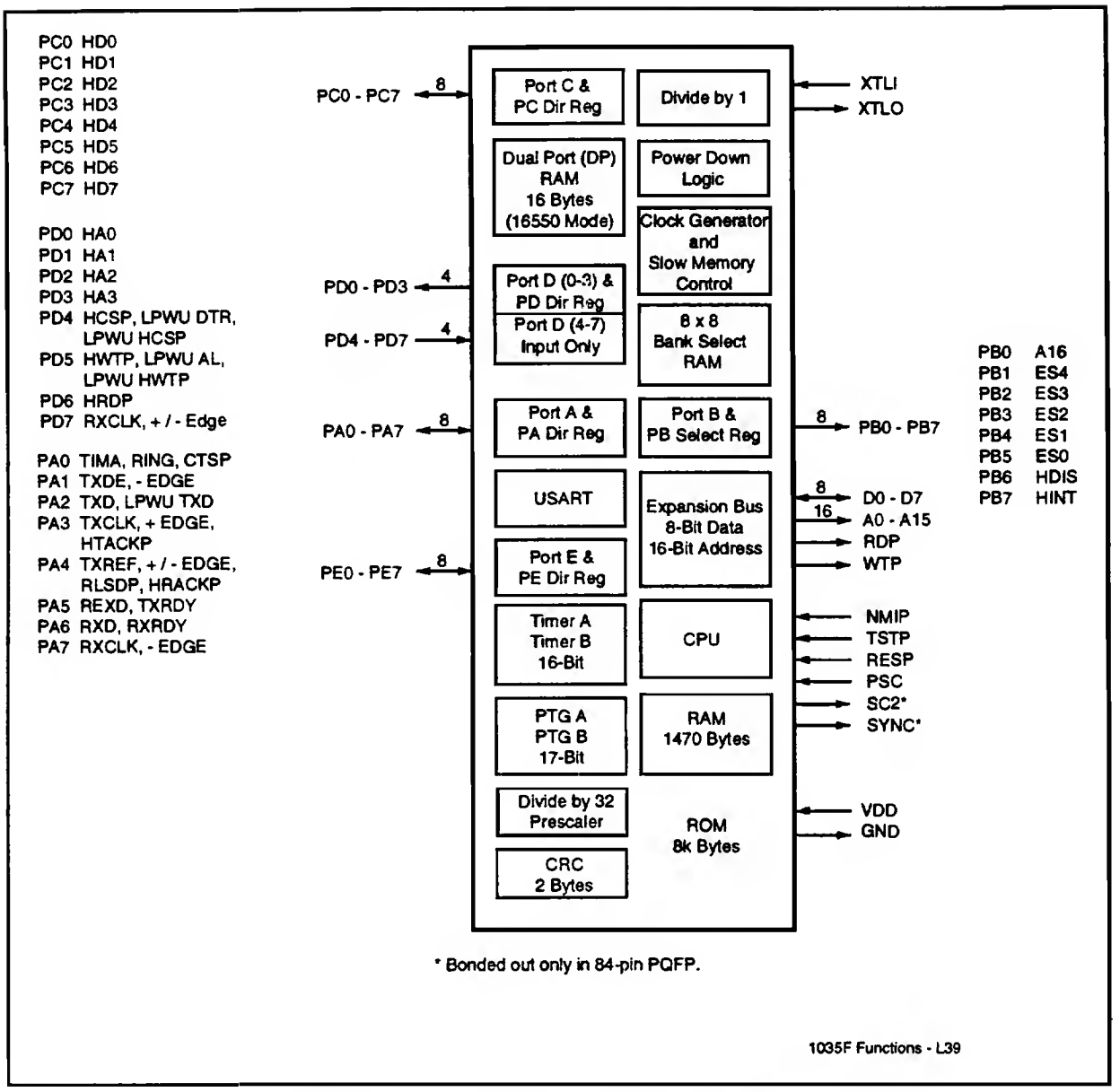

Figure 2-2b. Internal Functions and I/O Signals - L39

2.2. I/O PIN SIGNALS

The I/O pin signals are defined in Table 2-1.

Table 2-1. Interface Signal Description

Symbol	I/O	Name / Function
PA0-PA7	I/O	**General Purpose 8-Bit I/O Port A.** All pins can be assigned special functions under software control. The Port A Direction Register (PAD) must be set appropriately for all pins in both general and special use. PA1, PA3, PA4 and PA7 have edge detect circuitry that remains active regardless of data direction. PA3 and PA4 have an internal pull-ups (C40 and L3902 and subsequent).
TIMA (PA0)	I/O	**Timer A I/O.** An input in Timer A Event Counter or Pulse Width Measurement mode and an output in Timer A Pulse Generation mode.
RING (PA0)	I/O	**Ring.** An unclocked input whose positive level is used to clear the low power mode. Ring is enabled by LPR5.
CTSP (PA0)	I	**Clear To Send.** The negative edge of an external CTSP signal can be used to initialize the USART TXD synchronous mode word counter (SMR1 = 1).
TXDE (PA1)	O	**Serial Input Passthrough.** PA2 input is connected to the PA1 output when the serial pass through is selected (SFR7 = 1).
↓ Edge (PA1)	I/O	**PA1 Negative Edge Detect.** The PA1 edge detect flag (EIR7) is set on each detected edge and is cleared by writing a zero to register bit CI7. When the PA1 edge detect flag is set (EIR7 = 1), IRQ5 will be asserted if its enable is set (EIR4 = 1).
TXD (PA2)	I	**TXD Serial Input.** PA2 input is connected to the USART as the serial input stream when USART TXD mode is selected (SMR6 = 1).
TXCLK (PA3)	I/O	**TXCLK Clock.** PA3 is internally connected to the serial input clock when synchronous USART operation is selected (SMR4 = 1). TXCLK can be an external signal, an internal signal, or can be internally connected to TXREF (PA4). TXD is clocked on the rising edge of TXCLK.
∫ Edge (PA3/PA2)	I/O	**PA3/PA2 Positive Edge Detect.** The PA3/PA2 edge detect flag (SIR6) is set on each detected edge and is cleared by writing a zero to register bit CI3. When the PA3/PA2 edge detect flag is set (SIR6 = 1), IRQ4 will be asserted if its enable is set (SIR4 = 1). A PA3 edge is detected when SFR3 = 0 and a PA2 edge is detected when SFR3 = 1.
HTACKP (PA3)	I	**Host Transmit Acknowledge.** PA3 is an active low transmit acknowledge input signal asserting the host 16550 DMA TX FIFO address and chip select when host mode is enabled (HCR2 = 1), 16550/16450 DP RAM is selected (HCR1 = 1), FIFO is enabled which selects 16550 mode (FCR0 = 1), and serial mode is not selected (SMR7 = 0 and SMR4 = 0). Note that HTACKP on PA3 and HRACKP on PA4 are disabled when RXD mode is selected (SMR7 = 1) or SYNC mode is selected (SMR4 = 1) (C40 and L3902 and subsequent).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
TXREF (PA4)	I	**External TXD Reference Clock.** PA4 input is connected internally to PA3 output when synchronous USART operation is selected (SMR4 = 1) and TXREF is selected as the TXCLK source (SMR2 = 1).
↓ or ↑ Edge (PA4)	I/O	**PA4 Positive/Negative Edge Detect.** The PA4 edge detect flag (EIR6) is set on each detected edge and is cleared by writing a zero to register bit CI6. When the PA4 edge detect flag is set (EIR6 = 1), IRQ2 will be asserted if its enable is set (EIR3 = 1). PA4 will detect a negative (EIR1 = 0) or a positive (EIR1 = 1) edge.
RLSDP (PA4)	O	**Receiver Line Signal Detect.** The negative edge of an external RLSDP signal can be used to initialize the USART RXD synchronous mode word counter (SMR1 = 1).
HRACKP (PA4)	I	**Host Receive Acknowledge.** PA4 is an active low receive acknowledge input signal asserting the host 16550 DMA RX FIFO read address and chip select when host mode is enabled (HCR2 = 1), 16550/16450 DP RAM is selected (HCR1 = 1), FIFO is enabled which selects 16550 mode (FCR0 = 1), and serial mode is not selected (SMR7 = 0 and SMR4 = 0). Note that HTACKP on PA3 and HRACKP on PA4 are disabled when RXD mode is selected (SM7 = 1) or SYNC mode is selected (SM4 = 1) (C40 and L3902 and subsequent).
REXD (PA5)	I	**Serial Output Passthrough.** PA5 input is internally connected to the PA6 output when serial out pass through mode is selected (SMR7 = 1, SFR5 = 0, and SFR6 = 1).
TXRDY (PA5)	O	**Transmit Ready.** PA5 is an active high transmit ready output in the host 16550 DMA TX FIFO write mode and the 16450 mode when host mode is enabled (HCR2 = 1), 16550/16450 DP RAM is selected (HCR1 = 1), FIFO is enabled which selects 16550 mode (FCR0 = 1), and serial mode is not selected (SMR7 = 0 and SMR4 = 0). When asserted, TXRDY indicates that the TX FIFO is not full, i.e., the TX FIFO can accept data to be transmitted.
RXD (PA6)	O	**RXD Serial Output.** PA6 is connected as the USART serial output stream when RXD ON is selected (SMR7 = 1). When loopback is selected (SFR5 = 1) the PA2 signal is internally connected to the PA6 output. PA6 is also modified by the serial output pass through mode (SFR6 = 1).
RXRDY (PA6)	O	**Receive Ready.** PA6 is an active high receive ready output in the host 16550 DMA RX FIFO read mode and the 16450 mode when host mode is enabled (HCR2 = 1), 16550/16450 DP RAM is selected (HCR1 = 1), FIFO is enabled which selects 16550 mode (FCR0 = 1), and serial mode is not selected (SMR7 = 0 and SMR4 = 0). When asserted, RXRDY indicates that the RX FIFO is not empty, i.e., the RX FIFO has received data ready for transfer.
RXCLK (PA7)	I/O	**RXD Serial Output Clock.** PA7 output is internally connected to the USART in the synchronous mode (SMR7 = 1 and SMR4 = 1). RXCLK can be an external input signal or can be generated internally and become an output signal. Serial out is clocked on the negative edge of RXCLK.
↑ Edge (PA7)	I/O	**PA7 Negative Edge Detect.** The PA7 edge detect flag (SIR5) is set on each detected edge and is cleared by writing a zero to register bit CI4. When the PA7 edge detect flag is set (SIR5 = 1), IRQ6 will be asserted if its enable is set (SIR3 = 1).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
PB0-PB7	O	**General Purpose 8-Bit Output Port B.** All pins can be assigned special functions under software control. The Port B Selection Register (PBS) must be set appropriately for all pins in both general and special use. All Port B outputs float during reset active low.
A16 (PB0)	O	**A16.** When PBS0 = 0, the PB0 pin becomes the A16 address function from the selected or active (i) Banking RAM register bit 4 (BRi4). Note: PB0 is an A16 address option and may not be wire bonded out in some packages.
ES4 (PB1)	O	**ES4.** When PBS1 = 0, the PB1 pin becomes the ES4 chip select signal. ES4 is active low from addresses $0600 to $07FF.
ES3 (PB2)	O	**ES3.** When PBS2 = 0, the PB2 pin becomes the ES3 chip select signal. ES3 is controlled by bit 7 of the selected or active (i) Banking RAM register (BRi7).
ES2 (PB3)	O	**ES2.** When PBS3 = 0, the PB3 pin becomes the ES2 chip select signal. ES2 is controlled by bit 6 of the selected or active (i) Banking RAM register (BRi6). L39: Note that PB3 is a chip select option and may not be wire bonded out in some packages.
ES1 (PB4)	O	**ES1.** When PBS4 = 0, the PB4 pin becomes the ES1 chip select signal. ES1 is controlled by bit 5 of the selected or active (i) Banking RAM register (BRi5).
ES0 (PB5)	O	**ES0.** When PBS5 = 0, the PB5 pin becomes the ES0 chip select signal. ES0 is controlled by bit 4 of the selected or active (i) Banking RAM register (BRi4).
HDIS (PB6)	O	**Host Bus Driver Disable.** Active high output asserted when Host Mode is enabled (HCR2 = 1) and data is being read from the MCU host data bus. **Note:** It is recommended that the host bus I/O read and the chip select inputs to the MCU be ANDed and the output used as the host bus driver disable function instead of HDIS to control the host data direction through an external transceiver.
HINT (PB7)	O	**Host Bus Interrupt.** Active high output asserted in both the GP host interface (HC2 = 1 and HC1 = 0) or the 16450/16550 host interface (HC2 = 1 and HC1 = 1) under various conditions.
PC0-PC7	I/O	**General Purpose 8-Bit I/O Port C.** All pins can be assigned in a group to host bus data lines by a software option. The Port C Direction Register (PCD) must be set appropriately for all pins.
HD0-HD7 (PC0-PC7)	I/O	**Host Bus Data Lines.** PC0-PC7 are dedicated to the host bus interface bidirectional data lines HD0-HD7, respectively, when Host Mode is enabled (HCR2 = 1). The Port C direction register must be set to the output mode in this case (HCR2 = 1).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
PD0-PD3 PD4-PD7	I/O I	**General Purpose 4-Bit I/O and 4-Bit Input Port D.** PD0-PD3 are general purpose I/O pins while PD4-PD7 are input only. PD0-PD3 output latch is controlled by writing bits 0-3 at address $0003, while their direction control is contained in bits 4-7, respectively. PD0-PD6 are assigned in a group to host bus address and control lines when Host Mode is enabled (HCR2 = 1).
HA0-HA3 (PD0-PD3)	I	**Host Bus Address Lines.** PD0-PD3 are dedicated to the host bus interface as address lines HA0-HA3, respectively, when Host Mode is enabled (HCR2 = 1, HCR1 = 0). PD3 remains a GP pin in the 16450/16550 mode (HCR2 = 1, HCR1 = 1).
HCSP (PD4)	I	**Host Bus Chip Select.** PD4 is dedicated to the host bus interface as the active low chip select input when Host Mode is enabled (HCR2 = 1).
HWTP (PD5)	I	**Host Bus Write.** PD5 is dedicated to the host bus interface as an active low write control input when Host Mode is enabled (HCR2 = 1).
HRDP (PD6)	I	**Host Bus Read.** PD6 is dedicated to the host bus interface as an active low read control input when Host Mode is enabled (HCR2 = 1).
∫ or ⌊ Edge (PD7)	I	**PD7 Positive/Negative Edge Detect.** The PD7 edge detect flag (EIR5) is set on each detected edge and is cleared by writing a zero to register bit CI5. When the PD7 edge detect flag is set (EIR5 = 1), IRQ1 will be asserted if its enable is set (EIR2 = 1). PD7 will detect a negative (EIR0 = 0) or a positive (EIR0 = 1) edge.
PE0-PE7	I/O	**General Purpose 8-Bit I/O Port E.** The Port E Direction Register (PED) must be set appropriately for all pins.

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
A0-A12	O	**A0-A12 .** Address lines for external memory bus. These lines float during reset active.
A13-A15	O	**A13-A15 .** Address lines for external memory bus. These lines float during reset active. Address lines A13 - A15 are generated by bits 0 - 2 (m), respectively, of the active or selected (i) Banking RAM register (BRim).
D0-D7	I/O	**Expansion Bus Data .** D0-D7 provide an 8-bit bi-directional data bus for interfacing to external memories. D0-D7 float during reset active. L39: The receivers are automatically disabled during low power modes (Sleep and Stop)
WTP	O	**Expansion Bus Write.** Active low write strobe for the expansion bus. When WTP is asserted, data on the expansion data bus is written into the selected peripheral device. WTP remains high during MCU reset active.
RDP	O	**Expansion Bus Read.** Active low read strobe for the expansion bus. When RDP is asserted, data is read from the selected peripheral device onto the expansion data bus. RDP remains high during MCU reset active.
RESP	I	**Reset.** Active low input resets all MCU circuits and registers to their initial state. MCU operation resumes when the RESP input goes high; program execution starts at the location defined by the reset address vector.
NMIP	I	**Non-Maskable Interrupt.** Non- Maskable negative edge sensitive interrupt input. Interrupts program execution upon completion of current instruction and jumps to interrupt service subroutine starting at location defined by the NMI address vector.
LPWU NMIP	I	**Low Power Wake Up - NMIP.** When the MCU is in low power mode, a low level on the NMIP pin will cause normal operation to resume.
LPWU Ring (PA0)	I	**Low Power Wake Up - Ring .** When the MCU is in low power mode, a high level on PA0 will cause normal operation to resume if the Wake-Up Enable for PA0 (Ring) bit is set (LPR5 = 1).
LPWU HBW (PD4 + PD5)P	I	**Low Power Wake Up - Host Bus Write.** When the MCU is in low power mode, a low level on both PD4 and PD5 will cause normal operation to resume if the Wake-Up Enable for PD4 and PD5 (Host Bus Write and MCU Chip Select) bit is set (LPR4 = 1).
LPWU TXD (PA2)P	I	**Low Power Wake Up - TXD (TXD Start Bit).** When the MCU is in low power mode, a low level on PA2 will cause normal operation to resume if the Wake-Up Enable for PA2 (TXD Start Bit) bit is set (LPR3 = 1).
LPWU DTR (PD4)P	I	**Low Power Wake Up - DTR .** When the MCU is in low power mode, a low level on PD4 will cause normal operation to resume if the Wake-Up Enable for PD4 (DTR) bit is set (LPR2 = 1).
LPWU AL (PD5)P	I	**Low Power Wake Up - AL.** When the MCU is in low power mode, a low level on PD5 will cause normal operation to resume if the Wake-Up Enable for PD5 (AL) bit is set (LPR1 = 1).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
TSTP	I	**Emulator Mode.** The TSTP is an input with an internal pull-up. TSTP high places the MCU in the normal operating mode: 1. Internal ROM is enabled. 2. RDP and WTP reflect CPU activity. 3a. C40: Internal CPU read from pages 0, 1, 2, 3, or 4 (internal RAM and registers) do not cause the internal data to appear on the expansion bus. 3b. L39: Internal CPU read from pages 0, 1, 2, 3, 4, or 5 (internal RAM and registers) do not cause the internal data to appear on the expansion bus. TSTP low places the MCU in the emulation mode: 1. Internal ROM is disabled and all ROM fetches are transferred to the expansion bus. 2a. C40: Internal bus activity on pages 0, 1, 2, 3, or 4 impact D0-D7. Internal CPU read from pages 0-4 cause the internal data to appear on D0-D7. 2b. L39 Internal bus activity on pages 0, 1, 2, 3,4, or 5 impact D0-D7. Internal CPU read from pages 0-5 cause the internal data to appear on D0-D7.
SYNC	O	**Sync.** Sync high denotes that the current cycle is an op code fetch for the next instruction (Emulator package only.)
SC2	O	**SC2.** SC2 is an output operating at the crystal frequency or slower depending upon the external memory selected and is in phase with the internal C2 clock (Emulator package only.)
XTLI	I	**Crystal Oscillator Input Pin.** Input connection from crystal or external clock circuit.
XTLO	O	**Crystal Return.** Oscillator output connection to an external crystal. Open when the XTLI input is connected to an external clock.
PSC	I	**Power Supply Control (L39 Only).** Input pin with internal bond wire connected to internal pad to select either a VDD = 3.3 V device with 3.3 V I/O (logic 0) or a VDD = 5 V device with an internal 3.3 V regulator for low power operation of the core logic (logic 1). MOR0 reflects the RC pad. **5 V Part Only.** Input pin can be left unconnected (NC) or connected to VDD. **3.3 V Part Only.** Input pin with no external connection (NC). Note: If VDD = 5 V, the receivers will work only for CMOS. MOR0 reads logic-0.
MK6	NA	**Factory Option Pin - MK6.** Emulator only.
MK7	NA	**Factory Option Pin - MK7.** Emulator only.
VDD	I	**Power.** C40: +5 V. L39: +5 V or +3.3 V.
GND	I	**Ground.** Signal and power ground.